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WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

EXAMINER	
LUHRS, MICHAEL K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/735,518	MARTY ET AL.
	Examiner	Art Unit
	Michael K. Luhrs	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12 December 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Status of Claims

1. Applicant elected Group I, claims 1-7 in response dated 22 December 2004. Claims 8-9 were withdrawn by examiner to non-elected invention.

Specification

2. The Abstract of the disclosure is objected to because of the term "possibly", p. 12, line 6. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "possibly" in claim 1, line 4 is a relative term which renders the claim indefinite. The term "possibly" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim 1 recites the limitation "the thin wafer" in line 5. There is insufficient antecedent basis for this limitation in the claim. Examiner notes that claim 1, lines 3-4 identify a thin *semiconductor* wafer. Hence, if the thin wafer of line 5 is the same thin wafer of lines 3-4, then line 5 should read as the --thin semiconductor wafer--, or even, ~~the~~ said thin semiconductor wafer. Applicant is reminded to then carry the recommended correction, to the "thin wafer" of lines 6 and 9 of claim 1, which also lack antecedent, albeit are likely [to be] the same "thin wafer" as the "semiconductor thin wafer" of lines 3-4, hence these corrections would be similar to that presented above.

Claim 1 recites the limitation "forming connections between different areas" in line 8. There is insufficient antecedent basis for this limitation in the claim. Applicant expresses further limitation, to the "forming connections", i.e. in dependent claim 3, i.e. etching openings and filling the openings. There is however, no definitive connection being formed, i.e. from what? to what? Specifically, Claim 1 recites the limitation "between different areas" in line 8. There is insufficient antecedent basis for this limitation in the claim. Since no "areas" have been identified

previous to line 8, the examiner cannot further distinguish "different areas", and furthermore, therefore, cannot distinguish the locality of "between". Hence, in Claim 1 recitation of "between different areas" in line 8, has insufficient antecedent. While the applicant may be his own lexicographer and while the applicant might prefer to use the term *forming* connections as opposed to, say, *making* connections, no definitive connection has being identified, ...even if the examiner looks to claim 3, which etches openings and fills with conductive material, exactly what connection is being established? Examiner requests that the applicant indicate metes and bounds protection desired for the intended connection forming procedure. The examiner does not contend the phraseology, and also does not contend that the applicant prefers to identify the formed connection rather than 'from what' and 'to what', only contends that a resulting connection is not tangible. Assuming that the different areas of the rear surface of the thin wafer are chosen at random, then there is still no definitive relationship that a connection is formed "between different areas of the rear surface of the thin wafer" and the comprised steps of claim 3: that stipulates "etching and filling openings in an insulative layer", albeit because *that* insulative layer has not yet been identified with a forming step. Apparently the applicant is claiming the "forming connections" step in claim 1 with specific limitations in claim 3 for the forming connections, as being comprised of, "etching openings in an insulative layer formed on the rear surface of the thin wafer" formed in claim 3, hence the examiner looks to forming the insulative layer on the rear surface of the thin wafer, but cannot find it. i.e. Applicant says the insulative layer "formed" while the method step required is "forming", i.e. "ing", is the correct tense for the method step. Therefore, the actual step of forming the insulative layer of line 3, claim 3, is completely absent. Claim 1 lacks antecedent for forming the insulative layer which is related to the "forming connections" step of claim 1, since claim 3, the step of forming connections has some involvement with this insulative layer, it is never actually positively recited as being formed. Forming insulative layer is absent of a positively recited method step.

Hence, Claim 3 recites the limitation "in an insulating layer formed" in line 3. There is insufficient antecedent basis for this limitation in the claim. Claim 3 fails to actually recite the step of forming the insulative layer, as discussed above.

Claim 4, recites the step of "etching areas of reduced thickness" which the examiner does not understand. The etching can produce a reduction to the thickness, yet the claim states "of reduced thickness". Therefore there is

insufficient antecedent for "areas of reduced thickness" There are no reduced thickness areas previously defined, hence a step of etching *the* areas of reduced thickness cannot be performed.

Claim 4, recites "like said openings". Apparently the applicant is claiming that a comparison be made between said openings (of claim 3) and the areas of reduced thickness, i.e. that they be filled likewise. However it has been pointed out above that these areas of "reduced thickness" have not been identified. Therefore, and furthermore the comparison cannot be made. Yet, further, the examiner cannot fill an area of reduced thickness since there is no indication that the area being considered, is physically capable of being "filled". Examiner alleges that the step of etching areas of reduced thickness, may have been intended to read as --etching areas to reduce thickness, however does not contemplate how to correct the "filling of the reduced thickness", other than to suggest the area reduced, is replaced with a conductive material, viz, somehow, i.e. since there is no claim dependent on claim 4, the examiner cannot find any further limitations to indicate how this is done. Suggest correcting, that the etching is *to* reduce thickness and then clarify how the filler is to settle predominantly in that area.

Claim 5, recites "bottom of the openings" in line 5. There is insufficient antecedent basis for this limitation in the claim. There is no indication that the openings should or would have "bottoms". Also, "annealing to form the silicide" in line 5, *suggests* that a silicon be present to be annealed to form the silicide, as is required to form a silicide, assuming some interaction with the metal deposited in line 3, however there is no indication that a silicide be suddenly appropo to the annealing step. Examiner can only speculate that there is some silicon present, perhaps from the wafer. Please clarify the steps to form the silicide by expressing that the constituents of the silicide are in proximity, so that no speculation as to the sudden appearance of a silicide re generates. And also clarify, to show that the openings would in fact have bottoms.

Claim 5, recites "depositing a metal layer on the structure on the side of the insulating layer" yet such an insulating layer has not been properly set forth previously. Claim 5 is indefinite for the location of the insulative layer, because the insulative layer is not provided in the structure nor is it provided as having been set forth with a method step.

Claim 6, recites "after the step of filling the openings and possibly the areas of reduced thickness" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. There is no mention of "and possibly the areas of reduced thickness" in either of claim 3 or 1. Yet further, the examiner also notes that the term "possibly" is

a relative term which renders the claim indefinite. The term "possibly" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim 2, is indefinite for "wherein the thin wafer and the first support wafer are glued via an insulating wafer" because the applicant has provided the structure (emphasis added) of the first support wafer glued onto the thin semiconductor wafer (in claim 1), hence any further *method* limitation, such as might be presented as "via an insulating wafer" in claim 2, is moot, because the applicant has never initiated a gluing step in order to glue the first support wafer onto the thin wafer, thus cannot be via an insulating wafer. The applicant claims, in claim 1, of providing a structure, hence the applicant may certainly expand on what the *structure* is comprised of, but not a step to which further limits claim 1 with a further structural limitation, hence claim 2, fails to further limit claim 1 with a method step.

Claim 6, is indefinite for gluing a third support wafer on a second insulating layer, because claim 1, already recites that the third support wafer is glued on the "connections", hence claim 6 limitation allegedly contradicts.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

6. A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Gaul et. al. USPN 5,807,783 (hereinafter as "Gaul").

Regarding claim 1, Gaul teaches, *A method for manufacturing buried connections in an integrated circuit, comprising: providing a structure formed of a first support wafer glued onto a rear surface of a thin semiconductor wafer, one or several elements of the integrated circuit being possibly formed in and above the thin wafer; gluing a second support wafer on the structure on the front surface side of the thin wafer; removing the first support wafer; forming connections between different areas of the rear surface of the thin wafer; gluing a third support wafer on the connections; and removing the second support wafer*, as the following: the 'thin semiconductor wafer' as wafer

10 (line 5, column 4), having 'first support wafer', as handle wafer 12, (line 6, column 4), bonded thereto (see "bonded" in line 13, column 4). See Fig. 2, (albeit the applicant phraseology provides the *structure* and not the forming aspect of gluing the 1st support to the thin semiconductor wafer). Hence Gaul is prima facie for providing the structure. Nevertheless, Examiner further points out that bonded *is* considered *glued.* Next Gaul, is gluing the second support wafer in line 4, column 5, as second handle wafer, '40', as seen in Fig. 6. It can be seen that *one or several elements of the integrated circuit being possibly formed in and above the thin wafer,* because various elements are formed in wafer 10, from Figure 3 to Figure 5, as is taught by Gaul. The first support wafer, i.e. Gauls' handle wafer '12' is removed, in lines 36-37, column 5: See that, in Figure 7 handle wafer '12' is no longer present. In Figure 8, the wafer is inverted, thus Gaul is illustrating the connections into the wafer, (i.e. applicant's thin semiconductor wafer), elements 38, 36, in layer '14' of the wafer that Gaul formerly referred to as "10". There are connections in different areas of locations in layer '14' as seen in Fig. 8. Since the wafer is now shown inverted, the connections are of the rear side of the thin wafer, i.e. Gaul's wafer 10. The second support wafer is removed, i.e. Gaul removes his handle wafer 40 in line 32-33, column 6, as would those of the art. Gaul suggests that additional third support wafer would be forthcoming, since Gaul suggests the contacts 36 are compatible with multichip module manufacturing, external contacts connect the internal contacts to external electrical circuits (lines 53-55, column 5)...Examiner finds these suggestions to be sufficient for gluing the structure to another substrate that could be termed a third support wafer, see for example Fig. 10 preparation to attach to MCM (line 5, column 7).

Regarding claim 2, (Applicant provides the structure, the actual step of gluing the support wafet to the thin wafer has not been sufficiently been set forth by a gluing step, in claim 1, therefore the glued via an insulating wafer is not understood). Gaul teaches a oxide bond layer between wafer 10 and 12, is therefore an insulative wafer therebetween, (lines 14-15, column 4).

Regarding claim 3, Gaul teaches insulative layer 18 on wafer 10's backside. The insulative layer 18 has etched openings as vias formed there through (lines 45-48, column 4). Then filled with conductive material 35 as shown in Figure 5. Also Gaul forms insulative layer 30 comprises insulative material 31 (lines 51-52, column 4) through which connections are made within, see Fig. 5 connection 34, conductors, in layer 30. Hence connections are explicitly made as in lines 54, column 4 through to line 3, column 5.

Regarding claim 4, Gaul teaches that when removing wafer 12, (line 37, column 5), there can be an additional oxide deposited, this is on the rear side of wafer 10 now shown as 10 (prime), the actual oxide is not shown, yet inherently would be opened, as shown by the openings in layer 14 in Fig. 8. Apparently therefore the result of the removal of wafer 12 (from Fig. 6 to Fig. 7) reveals etch stop layer 14, hence as an etch stop is invariably reduced in thickness, is thus filled with '38' and '36' i.e. conductive material such as silicide as in line 48, column 5.

Regarding claim 5, Gaul teaches depositing a metal layer, as conductive layer 33, (conductive layer is considered broader than the type of conductive layer, i.e. metal would considered . in the openings 32 in Fig. 5 (lines 48-49, column 4). Gaul also teaches the metal interconnects, discussed above, and that selected portions of the contacts 36 can be silicided (lines 48-49, column 5). Since contacts '38' are at the vias '32', the wafer inverted, hence the silicide is at the via bottom, albeit now the wafer top as seen in Fig. 8. Gaul lacks expressly annealing, yet it is well within the skill of one having ordinary skill in the art to supply a silicide by annealing the appropriate constituents that comprise a silicide.

Regarding claim 6, Gaul teaches chem.-mech polishing in line 38, column 5 a second insulative layer can be the oxide expressed in line 42, column 5, hence when bonded to an MCM, such an MCM is considered herein to be applicant's third support wafer.

Regarding claim 7, Gaul teaches that the second support wafer (i.e. Gauls second handle wafer 40) is bonded to the ineterconnect layer 30, hence Gaul's layer 30 is a bonding layer covering the structure, i.e. bond layer 30 is on the structure comprised of: wafer 10 (now 10 prime) and wafer 12, as seen in Fig. 5, prior to, adding the 2nd support wafer 40 as seen in Fig. 6. Hence second support wafer 40, is bonded via bond layer 30 to the structure as indicated by the arrows in Figure 6.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael K. Luhrs whose telephone number is 571-272-1874. The examiner can normally be reached on M-F, 8-5.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MKL
Michael K. Luhrs
3/18/05

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800